We Claim:

Sub #17

1. A method for improving resolution of a current mode driver, where the current mode driver is operable to provide an output that falls within a predetermined range, the method comprising the steps of:

sensing at least one of a process condition, a voltage condition and a temperature condition;

adjusting a full scale current of a DAC in accordance with the sensing step; and

setting a current control signal based on an output of the DAC.

2. A method for improving resolution of a current mode driver as claimed in claim 1, wherein the step of adjusting the full scale current comprises the steps of:

generating an adjustment signal in response to the sensing step; and

applying the adjustment signal to the current mode driver, the adjustment signal causing the current mode driver to adjust the full scale current.

3. A method as claimed in claim 2, wherein the step of applying the adjustment signal to the current mode driver comprises applying at least one predetermined voltage to a corresponding at least one transistor switch.

4. A method for improving resolution of a current mode driver as claimed in claim 1, wherein the current control signal comprises a plurality of bits.

5. A method as claimed in claim 1, wherein the sensing step comprises determining a condition associated with a phase-locked loop.

6. A method as claimed in claim 1, wherein the sensing step comprises determining a condition associated with a delayed locked loop.

7. A method as claimed in claim 1, wherein the sensing step comprises the steps of:

applying a PVT independent current to a PVT sensitive load; and

detecting a voltage drop across the PVT sensitive load.

8. A method as claimed in claim 1, wherein the sensing step comprises the steps of :

applying a pulse to a delay line and a first plurality of latches, wherein the delay line comprises a second plurality of delay stages;

coupling an output of a subset of the plurality of delay stages to an input of a corresponding latch from the plurality of latches; and

decoding an output from the plurality of latches.

9. A method as claimed in claim 1, wherein the sensing step comprises sensing a PVT sensitive DC parameter.

10. A method as claimed in claim 1, wherein the sensing step comprises sensing a PVT sensitive AC parameter.

11. In a current mode driver that is operable to provide an output that falls within a predetermined range, wherein the output is set in accordance with a current control signal, a method of improving resolution of the current mode driver, the method comprising the steps of:

applying the current control signal to cause the current mode driver to sink a full scale current;

providing a PVT detector to sense a characteristic that comprises at least one of a process condition, a voltage condition and a temperature condition;

generating a full scale current adjustment signal at the PVT detector; and

applying the full scale current adjustment signal to alter the full scale current of the current mode driver.

12. A method of improving resolution of a current mode driver as claimed in claim 11, wherein the step of applying the full scale current adjustment signal comprises coupling the adjustment signal to a digital-to-analog converter.

13. A method of improving resolution of a current mode driver as claimed in claim 12, wherein the adjustment signal is a two-bit signal and the digital-to-analog converter has at least two inputs.

14. A method of improving resolution of a current mode driver as claimed in claim 12, wherein the digital-to-analog converter provides an output signal in response to the adjustment signal.

15. A method of improving resolution of a current mode driver, comprising the steps of:

applying a first current control signal to a digital-to-analog converter, the digital-to-analog converter providing a first output in response thereto;

applying the first output as a gate voltage to control a full scale current of an output driver

calibrating the output driver by comparing a second output, which is provided by the output driver, with a reference; and

augmenting the first current control signal when the second output differs from the reference.

16. A method as claimed in claim 15, wherein the step of calibrating the output driver comprises deriving the second output from a signal provided directly by the output driver.

17. A method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a resistive divider.

18. A method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a transconductance stage.

19. A method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a switched capacitor circuit.

20. A method as claimed in claim 15, wherein the first current control signal is applied under user control.

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